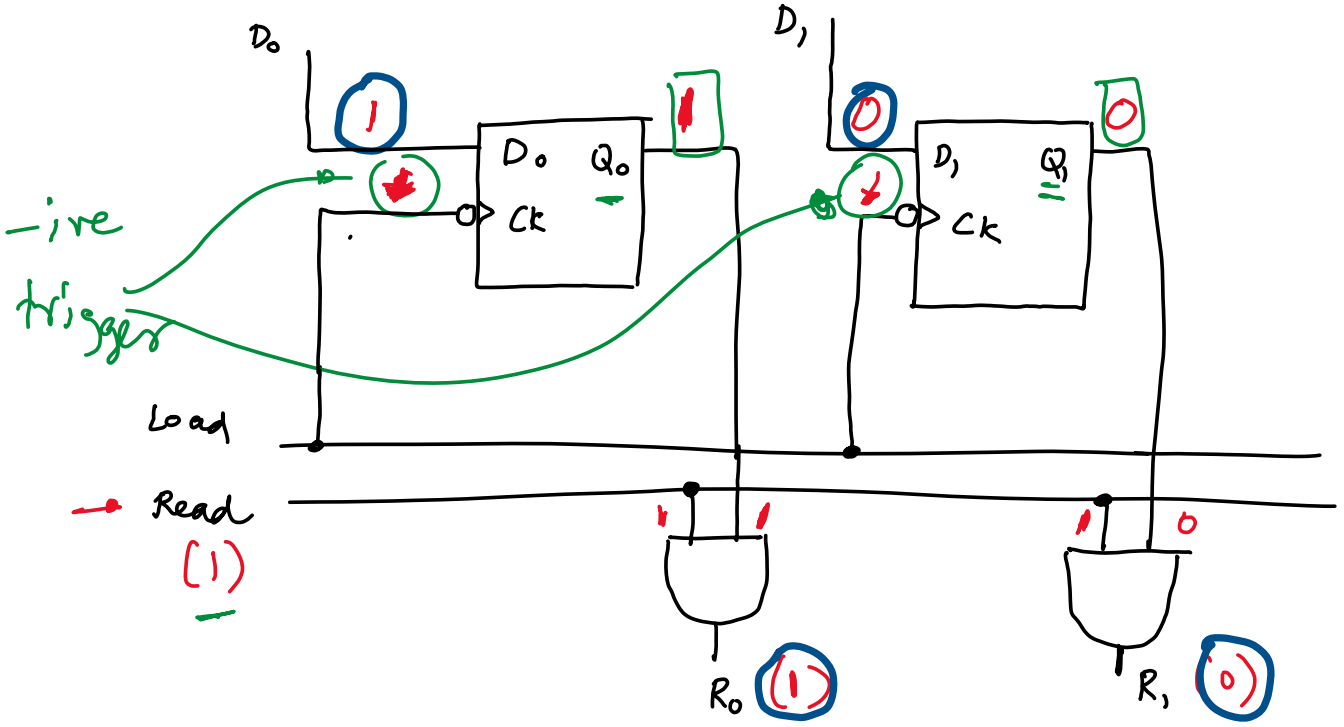
① Data Register

Example : 2 Bit Data register



D	Ck	Q	$\bar{Q}$
0	↓	0	1
1	↓	1	0
X	0,1,↑	Q_0	$\bar{Q}_0$

Used to hold data for arithmetic calculations

Let us assume $D_0 = 1$; $D_1 = 0$ (inputs)

When CK ↓

$Q_0 = 1$; $Q_1 = 0$ — Holds this o/p.

Setting Read = 1

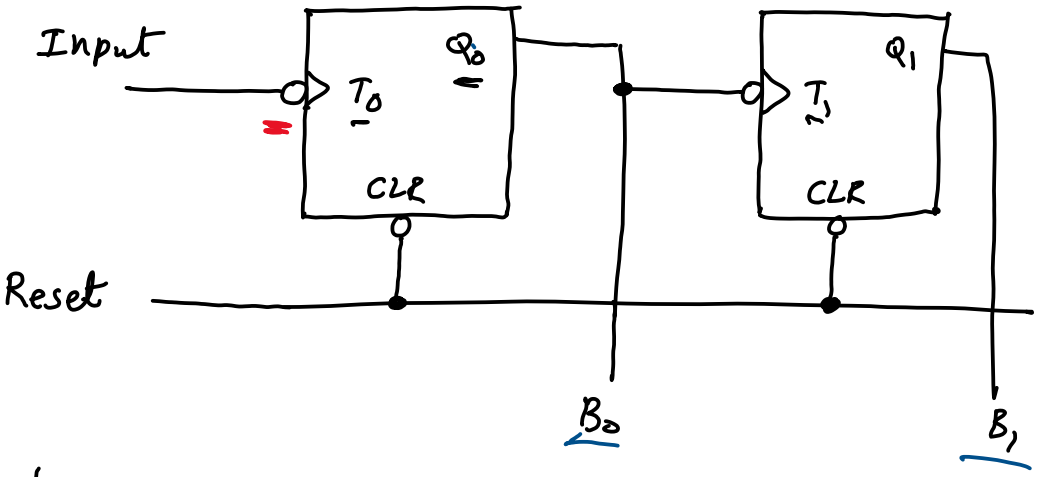
$R_0 = 1$ $R_1 = 0$

data

Register function → output = input

② Binary counter

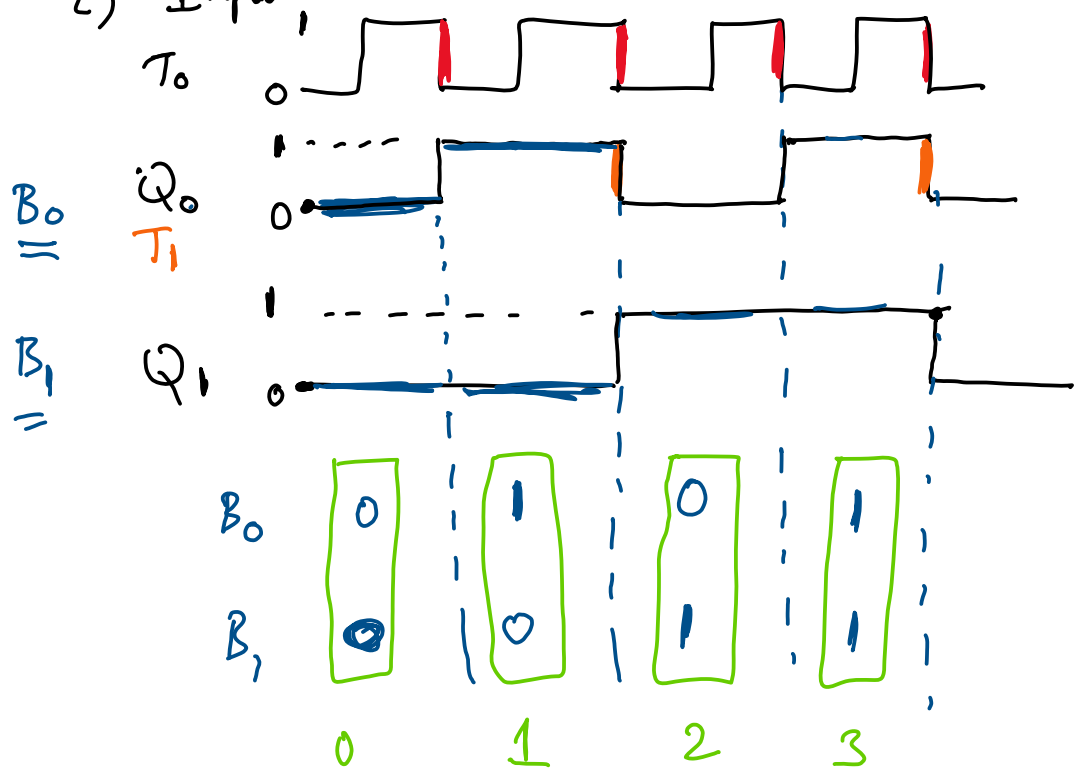
Example: 2 bit counter. It counts 0, 1, 2, 3. n Flip Flops will enable counting upto $2^n - 1$



T	Q
↓	$\bar{Q}$
0, 1, ↑	Q

1) Reset = 1 set $B_0 = B_1 = 0$

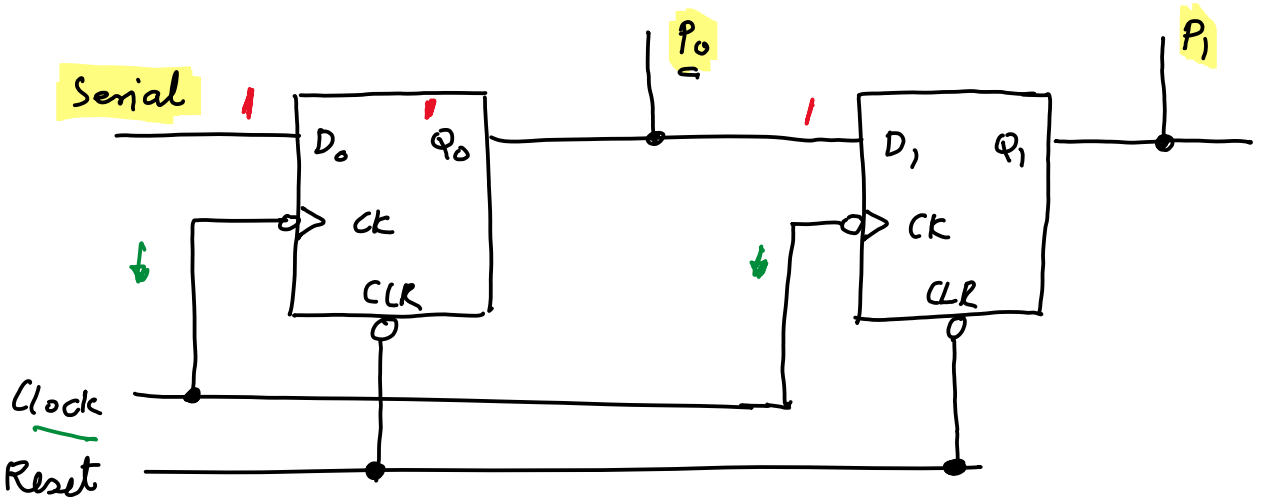
2) Input



③ Serial to parallel converter

one input (serial) ⟶ multiple outputs (parallel)

Example: Two 2D Flip Flops to convert serial data to Two output streams.



D	CK	Q	$\bar{Q}$
0	↓	0	1
1	↓	1	0
X	0, 1, ↑	Q_0	$\bar{Q}_0$

0 / 1

1) Reset = 1 (if needed)

2) Serial = 1 $P_0, P_1 = ?$

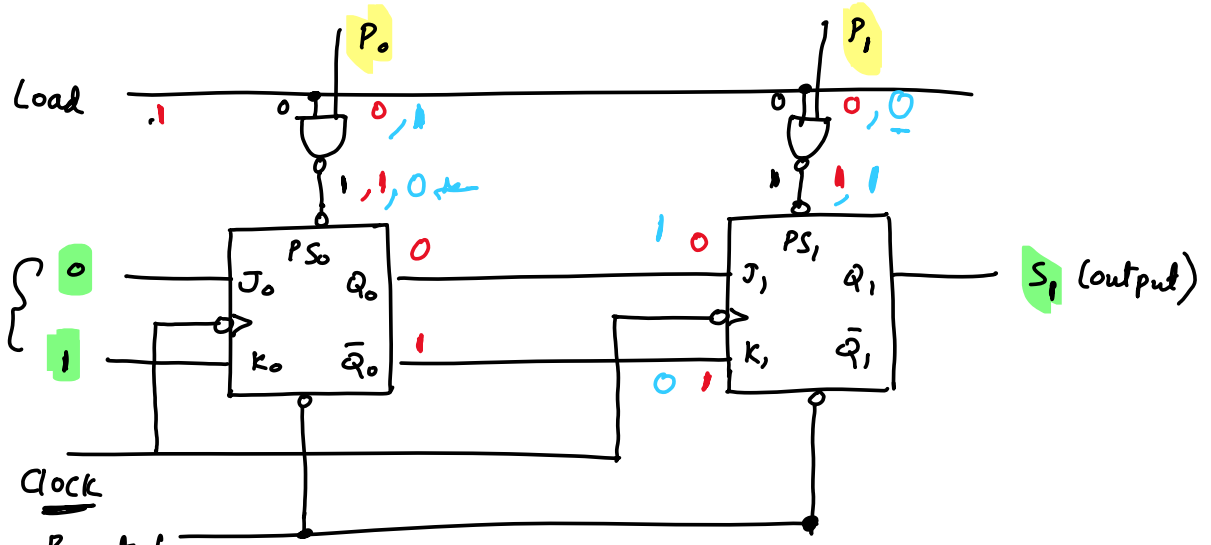
$Q_0 = 1$ $Q_1 = 1$

$P_0 = 1$ $P_1 = 1$

3) Use similar logic for Serial = 0.

④ Parallel to Serial converter

2 or more inputs ⟶ 1 output (serial)



Preset	Clear	CK	J	K	Q	$\bar{Q}$	
0	1	X	X	X	1	0	Init.
1	0	X	X	X	0	1	
1	1	↓	1	0	1	0	
1	1	↓	0	1	0	1	
					↑		

1) Load = 0 ; $PS_0 = PS_1 = 1$
$Q_0 = 0$, $Q_1 = S_1 = 0$
Flip-Flop is Reset

2) Normal operations
CLR = 1, Load = 1
when CK ↓

There are 4 cases.

i) $P_0 = P_1 = 0$. Since $J_0 = 0$; $K_0 = 1$ ⟶ $Q_0 = J_1 = 0$
$\bar{Q}_0 = K_1 = 1$
$Q_1 = 0 = S_1$

ii) $P_0 = 1$, $P_1 = 0$ $PS_0 = 0$; $PS_1 = 1$

Since $J_0 = 0$ $Q_0 = 1 = J_1$
$K_0 = 1$ $\bar{Q}_0 = 0 = K_1$

$Q_1 = 1 = S_1$
$\bar{Q}_1 = 0$

(iii) $P_0 = 0,\ P_1 = 1$ figure this out at home

$S_1 = 1$

(iv) $P_0 = 1,\ P_1 = 1$ $S_1 = 1$

Thus $S_1 = 1$ as long as one of P_0 or $P_1 = 1$