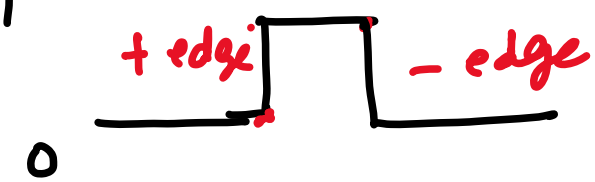
Sequential logic

Here the timing or sequencing of the input signals is important

e.g. Flip-Flops, counters, latches, microprocessors.

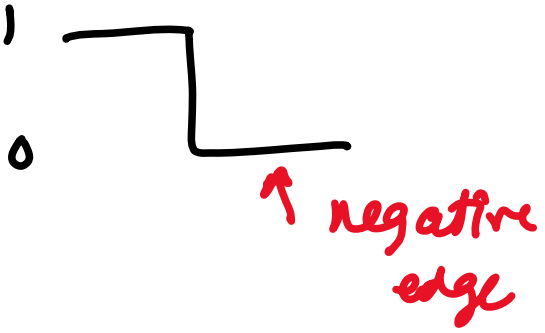
Sequential logic responds to inputs only when a separate trigger signal transitions from one level to another this trigger is the CLOCK (CK) signal

Clock pulse edges



positive edge triggered

Negative edge triggered



Two types of edge triggered devices

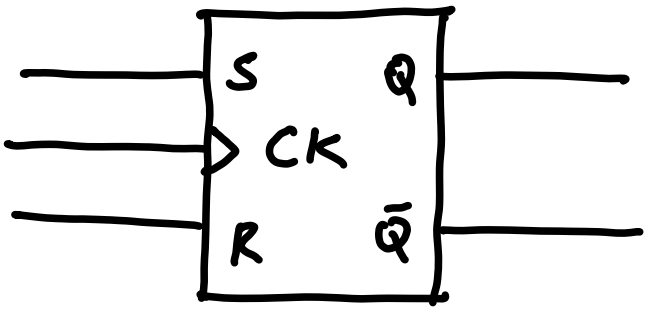
1) Positive edge triggered CK = 1
2) Negative edge triggered CK = 0

↑ Input to Sequential logic gates

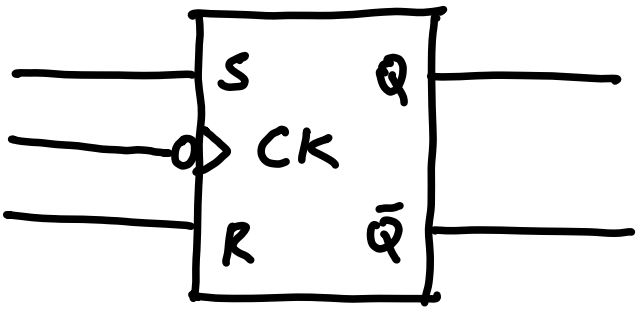
Flip-Flops

Is a sequential logic device that can store data and switch between states (0/1).

① RS Flip-Flop



Positive edge-triggered



Negative edge-triggered.

Inputs
- S: set pin
- R: reset pin

Outputs
- Q, $\bar{Q}$

▷ CK: Clock / positive edge-trigger

○▷ CK: Clock / Negative edge-trigger

There are 2 aspects to Flip-Flop

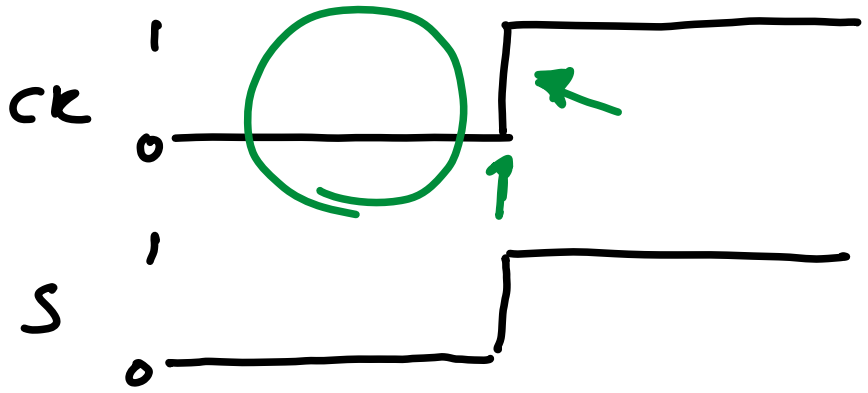
① Truth Table

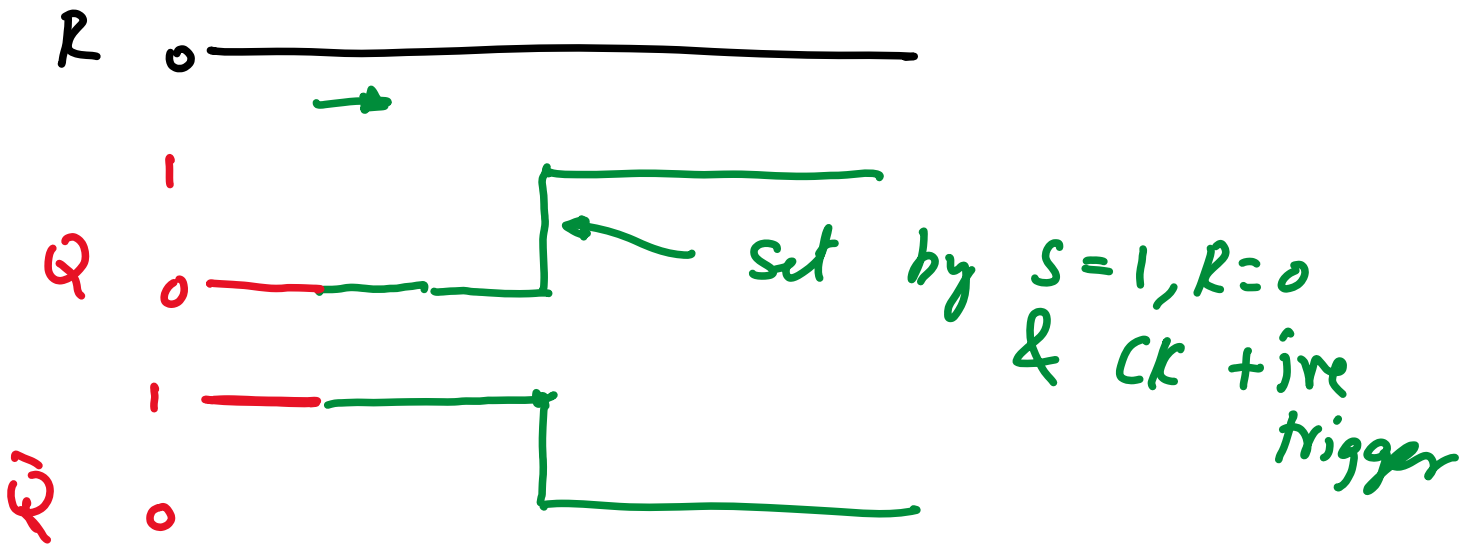
S	R	Q	$\bar{Q}$	Comments
0	0	Q_0	$\bar{Q}_0$	output Q is unchanged
1	0	1	0	Set
0	1	0	1	Reset
x	x	Not available		R = S = 1 not allowed.

② The output Q, $\bar{Q}$ will change when S, R are changed ONLY when CK or CLOCK has the correct trigger

Illustration

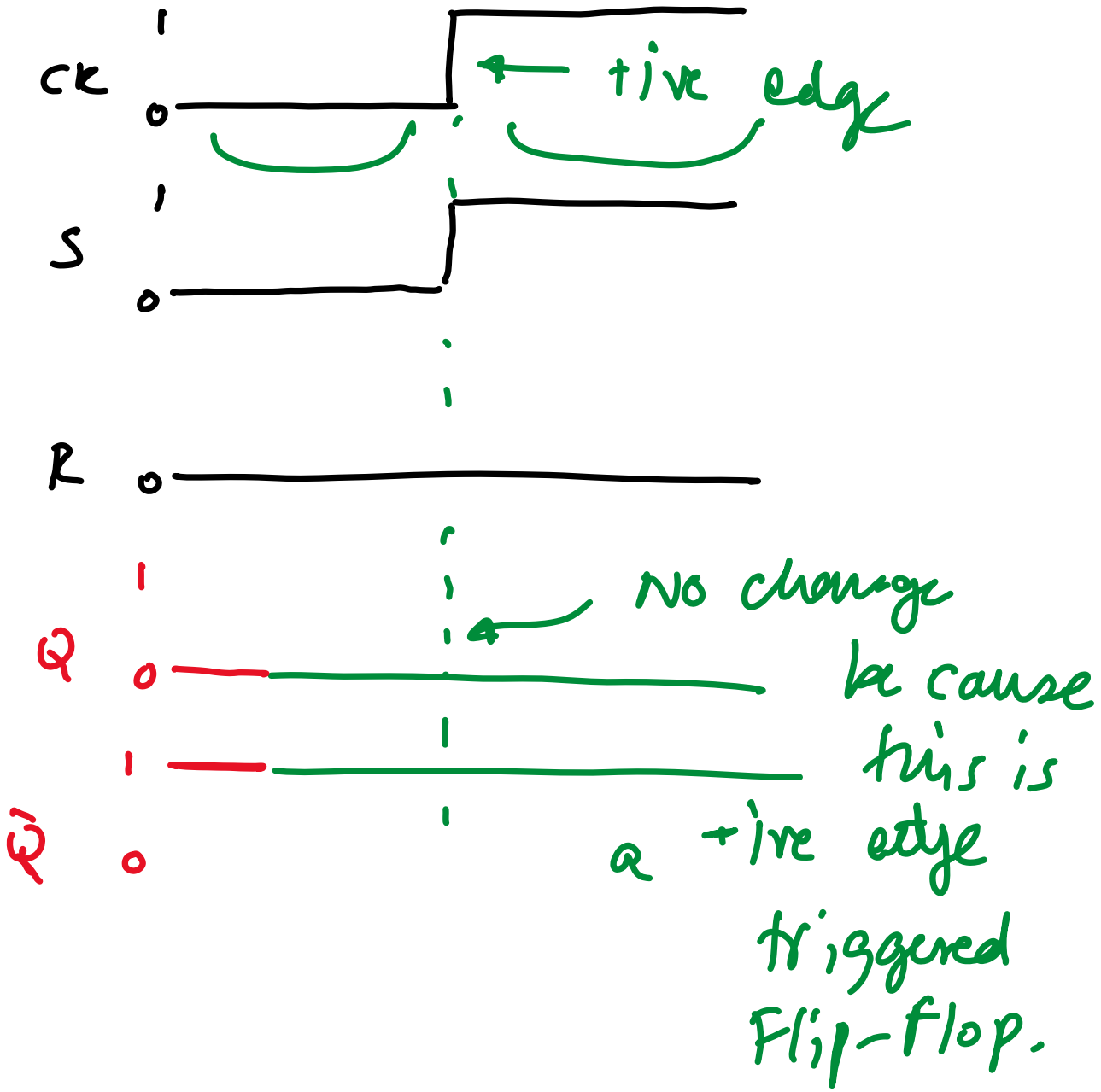
Case 1 Positive edge triggered RS Flip-Flop. It is in the state $Q = 0 / \bar{Q} = 1$





Illustration

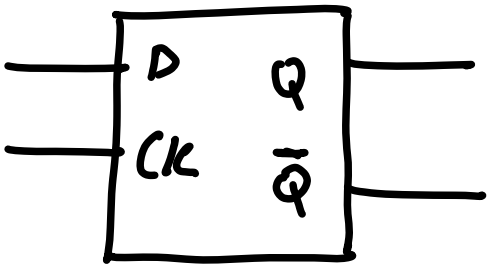
Case 1 Negative edge triggered RS Flip-Flop. It is in the State $Q = 0 / \bar{Q} = 1$



Latch

Is a level triggered flip-flop.

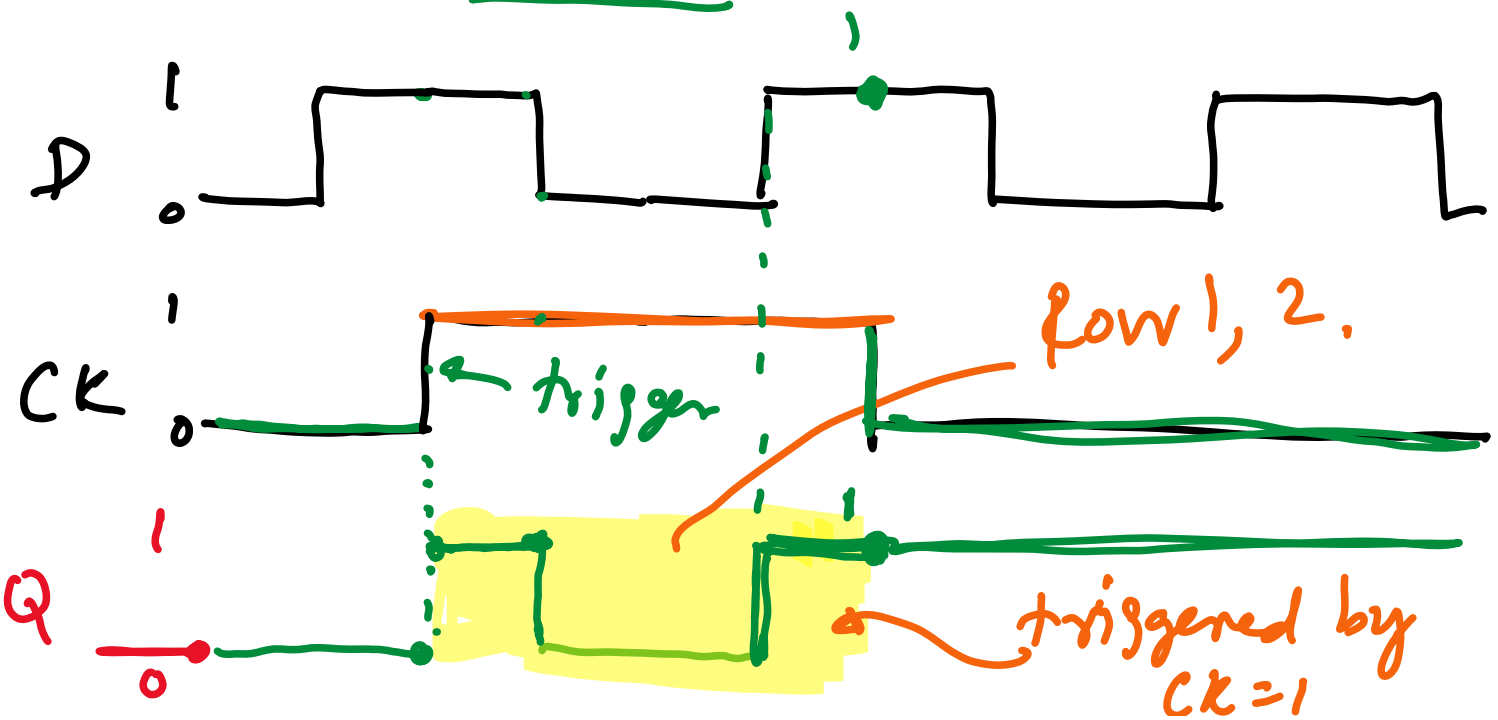
└ 0 or 1



D	CK	Q	$\bar{Q}$
0	↑	0	1
1	↑	1	0
X	0, ↑, ↓	Q_0	$\bar{Q}_0$
(0,1)		output unchanged	

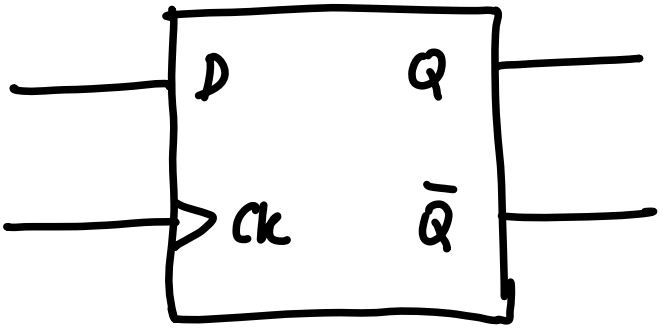
Positive level

Example: Positive level trigger




Ck=1

D Flip-Flop



positive-edge trigger

D	Ck	Q	$\bar{Q}$
0	↑	0	1
1	↑	1	0
X	0, 1, ↓	Q_0	$\bar{Q}_0$

X: 0 or 1

④ JK Flip-Flop

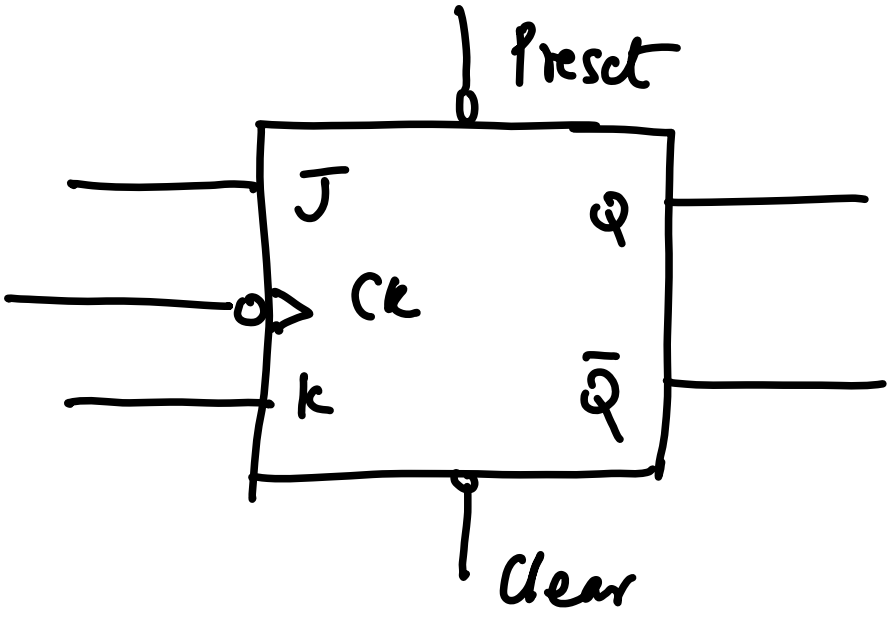
~ similar to RS Flip-Flop

JK in place of RS

~ R & S cannot be high simultaneously

J & K can be high "

~ Preset & Clear pin to initialize the state



5 inputs J, K, Ck, Preset, Clear.

2 outputs Q, $\bar{Q}$

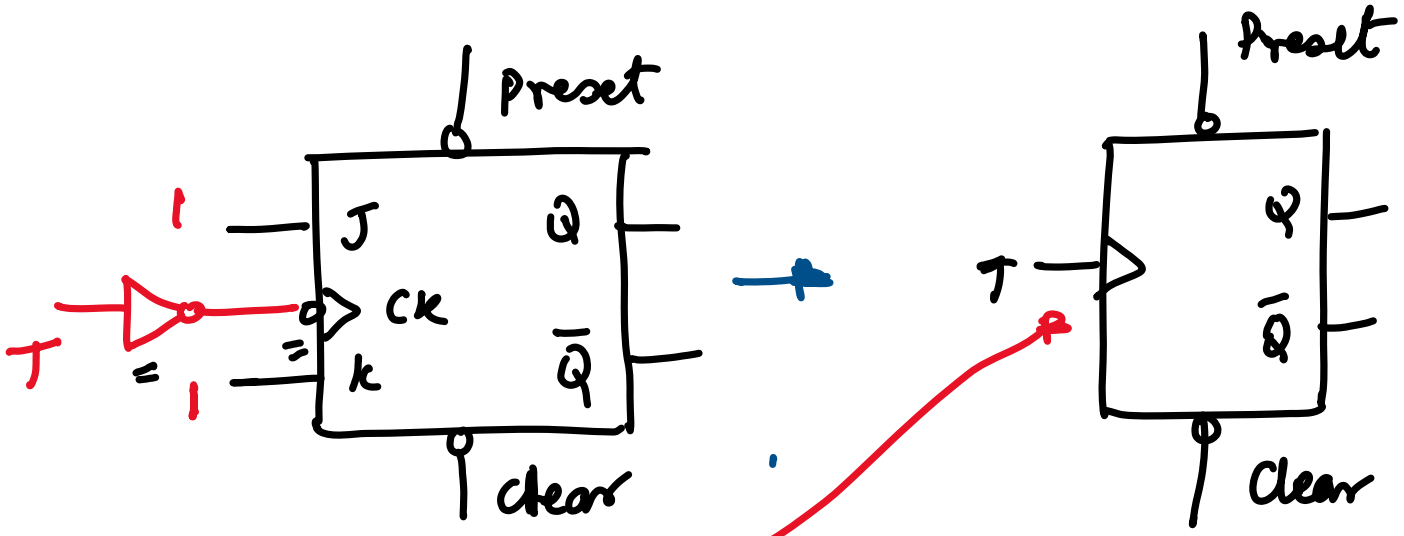
$\overline{\text{Preset}}$	$\overline{\text{Clear}}$	Clk	J	K	Q	$\bar{Q}$	
0	1	X	X	X	1	0	} Initialize
1	0	X	X	X	0	1	
0	0	— Not available —					Not Permitted
1	1	↓	0	0	Q_0	$\bar{Q}_0$	} Useful Inputs
1	1	↓	1	0	1	0	
1	1	↓	0	1	0	1	
1	1	↓	1	1	$\bar{Q}_0$	Q_0	
1	1	↑, 0, 1	X	X	Q_0	$\bar{Q}_0$	Unchanged

Incorrect trigger

0/1

All Flip-Flops can be constructed using JK Flip-Flops.

T or Toggle Flip-Flop



tive edge

T	Preset	Clear	Q	$\bar{Q}$	
↑	1	1	$\bar{Q}_0$	Q_0	toggle
= 0, 1, ↓	1	1	Q_0	$\bar{Q}_0$	unchanged
0, 1, ↓, ↑	0	1	1	0	} Initialize
0, 1, ↓, ↑	1	0	0	1	

Does not depend on these inputs