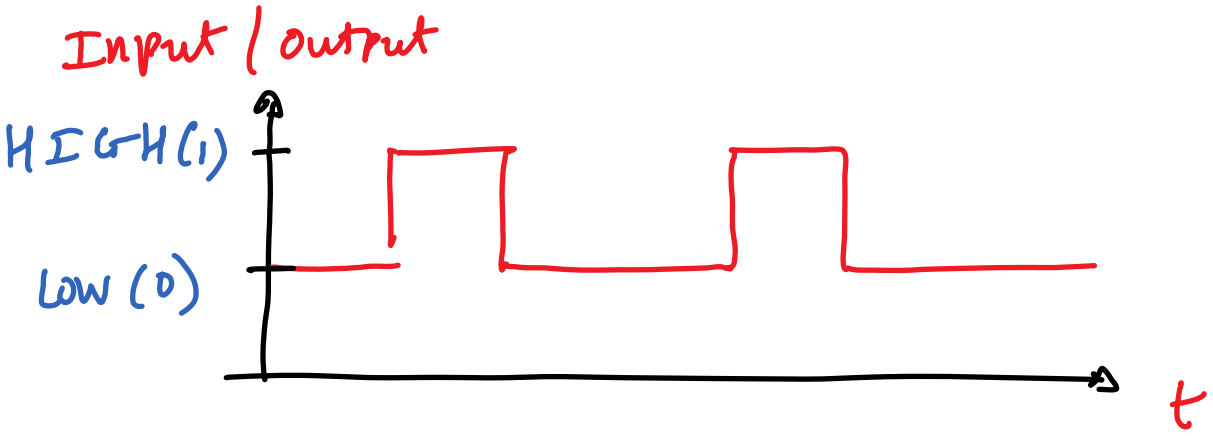
Digital signals and circuits



① Combinational logic

Outputs are function of instantaneous inputs (e.g. Gates (AND, OR, ...)

② Sequential logic

Output depends on history of inputs (e.g. Flip-Flops)

Digital Representation

Example: 523_{10}

$= 500 + 20 + 3$

$= 5(10^2) + 2(10^1) + 3(10^0)$

5	2	3

EXample: 100_2

$= 1(2^2) + 0(2^1) + 0(2^0)$

$= 4 + 0 + 0$

$= 4_{10}$

100 → least significant Bit (LSB)

↑ Most significant Bit (MSB)

Bit ⟶ 0 or 1 ; BYTE – 8 bits.

Hard Drive: 2 TB = 2 Tera Byte

$= 2(10^{12})$ Bytes

$= 2(10^{12})$ 8 bits

$= 16(10^{12})$ bits

$= 1.6(10^{13})$ bits

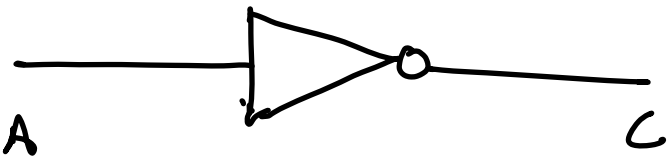
Base 8 system (Octal)

Base 16 system (hexadecimal)

Combinational Logic Gates

We will look at 6 Logic gates.

① Inverter or NOT gate



input output

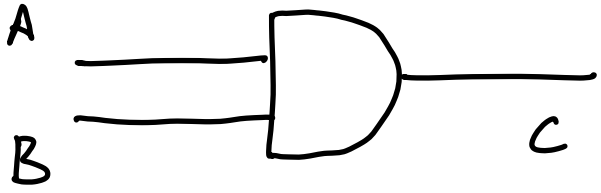
Expression

$C = \overline{A}$

Truth Table

A	C
0	1
1	0

② AND Gate



Expression

$C = A \cdot B$

multiply

Truth Table

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

if (X AND y)

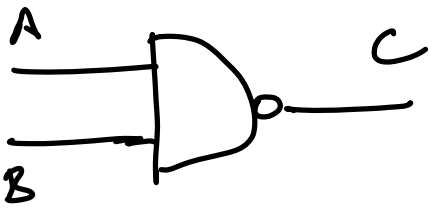
both should be true

for if condition to be true

③ NAND

Expression

$C = \overline{A \cdot B}$

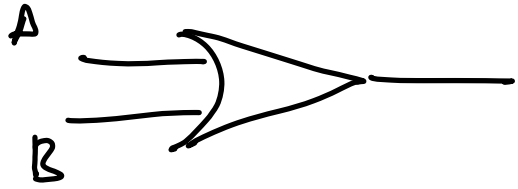


Truth Table

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

④ OR

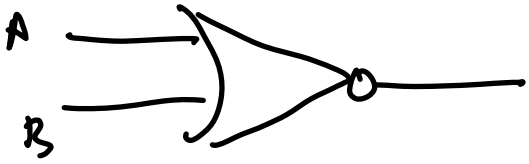
$C = A + B$



A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

⑤ NOR

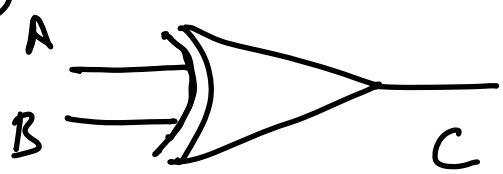
$C = \overline{A + B}$



A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate

⑥



Expression

$C = A \oplus B$

$= A \cdot \bar{B} + \bar{A} \cdot B$

$1 \cdot 1$

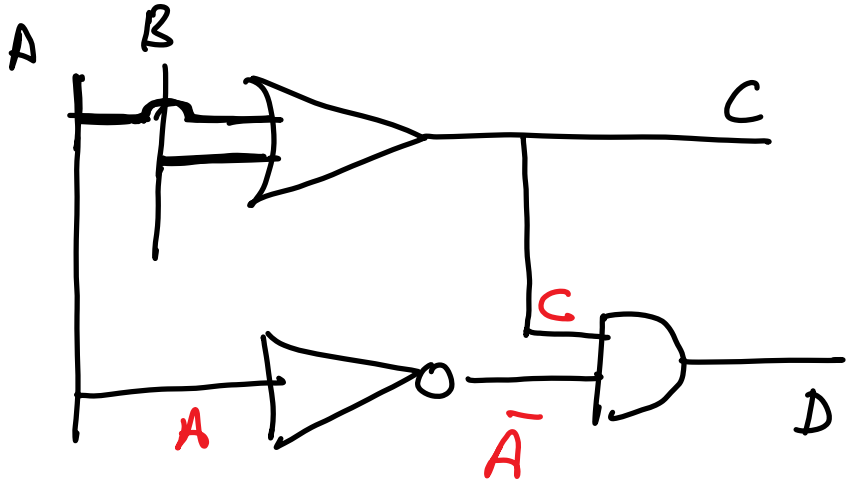
Truth Table

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Logic gates are available as IC's

↳ made up of resistors, capacitors, BJT's

EXAMPLE 1



(1) Write a boolean expression for C and D in terms of A and B

(2) Draw the truth table

---

(1) $C = A + B$

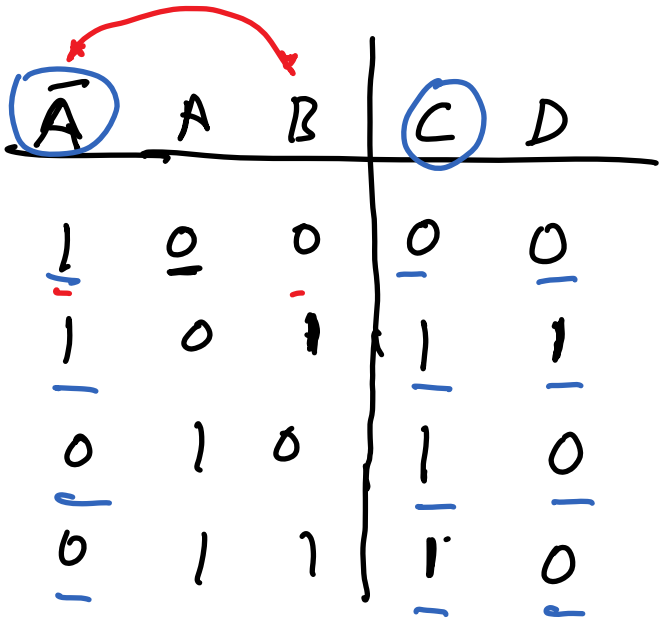
$$D = C \cdot \bar{A} = (A+B) \cdot \bar{A} = \bar{A} \cdot (A+B)$$

$$= \cancel{A \cdot A} + \bar{A} \cdot B = \bar{A} \cdot B$$

Truth table

$C = A + B$

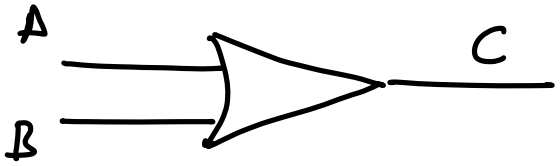
$D = \bar{A} \cdot B = C \cdot \bar{A}$



$\bar{A}$	A	B	C	D
1	0	0	0	0
1	0	1	1	1
0	1	0	1	0
0	1	1	1	0

Timing diagram

Example

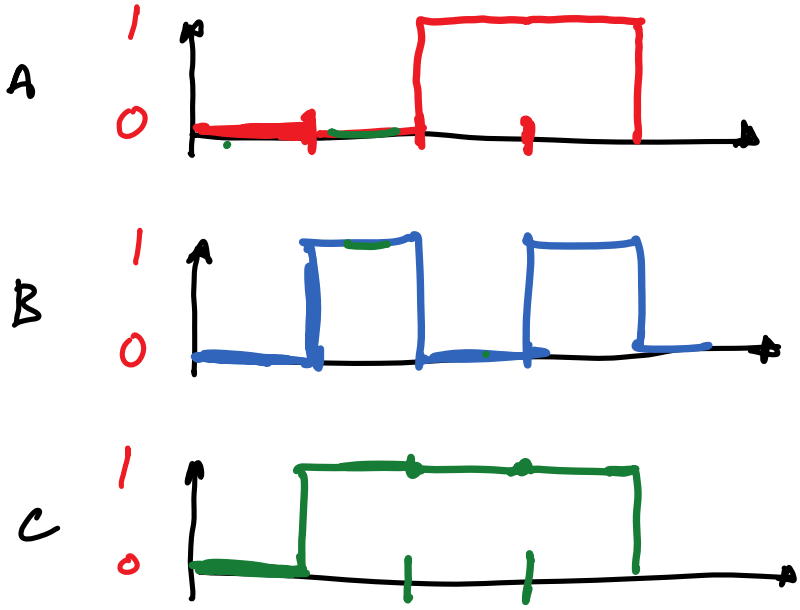


$C = A + B$

input output

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Timing diagram: Truth table as a plot



Timing diagram can be obtained using

① multi-input oscilloscope

② logic analyzer